

Notice of References Cited	Application/Control No. 10/711,953	Applicant(s)/Patent Under Reexamination CLINE ET AL.	
	Examiner Eric B. Chen	Art Unit 1765	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,380,095	04-2002	Liu et al.	438/719
	B	US-6,653,734	11-2003	Flanner et al.	257/758
	C	US-6,180,533	01-2001	Jain et al.	438/719
	D	US-6,127,278	10-2000	Wang et al.	438/719
	E	US-6,727,158	04-2004	Sundt et al.	438/424
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	M	US-			

FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Streetman, Solid State Electronic Devices, 1990, Prentice Hall, 3rd ed., p. 332.
	V	Wolf et al., Silicon Processing for the VLSI Era, 1986, Lattice Press, Vol. 1, pp. 514-515.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
 Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.